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Application Number	Not Yet Assigned
Filing Date	02/13/2004
First Named Inventor	Yi-Hsun Wu
Art Unit	Not Yet Assigned
Examiner Name	Not Yet Assigned
Attorney Docket Number	N1085-00190

[illegible]

Examiner Signature		Date Considered	3-2-06
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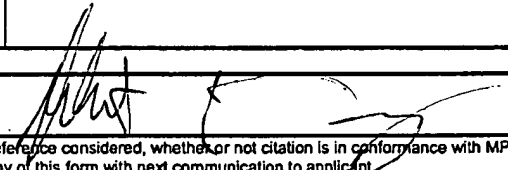
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Substitute for form 1449/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (Use as many sheets as necessary)		<b>Complete if Known</b>	
		Applicant Number	Not Yet Assigned
		Filing Date	2/13/2004
		First Named Inventor	Yi-Hsun Wu
		Art Unit	Not Yet Assigned
		Examiner Name	Not Yet Assigned
Sheet 2	of 2	Attorney Docket Number	N1085-00190

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
RTD	D	MING-DOU KER ET AL., "Complementary-SCR ESD Protection Circuit with Interdigitated Finger-Type Layout for Input Pads of Submicron CMOS IC's",	
FTD		IEEE Transactions On Electron Devices, Vol. 42, No. 7, July 1995, Pages 1297-1304	
RTD	E	MING-DOU KER ET AL., "A Gate-Coupled PTLSCR/NTLSCR ESD Protection Circuit for Deep-Submicron Low-Voltage CMOS IC's", IEEE Journal Of Solid-State Circuits, Vol. 32 No. 1 January 1997 Pages 38-51	
RTD	F	CHRISTIAN C. RUSS ET AL., "GGSCRs: GGNMOS Triggered Silicon Controlled Rectifiers for ESD Protection in Deep Sub-Micron CMOS Processes", 2001 EOS/ESD	
RTD		Symposium, 10 pages	
RTD	G	MARKUS P.J. MERGENS ET AL., "High Holding Current SCRs (HHI-SCR) for ESD Protection and Latch-up Immune IC Operation", 2002 Sarnoff and ESD Association,	
		Pages 1-8	

Examiner Signature		Date Considered	3-02-06
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